UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,494	02/06/2002	Taeg-Hyun Kang	40013.001	1924

27966 7590 08/19/2004

KENNETH E. HORTON
KIRTON & MCCONKLE
60 EAST SOUTH TEMPLE
SUITE 1800
SALTLAKE CITY, UT 84111

EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,494	KANG ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *11-18 and 30-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,19-29,40 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 40 and 41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The invention shows a thick gate insulator in Figure 2 #170 and the disclosure discloses a gate insulator, but claims 40 and 41 are teaching the invention without a gate insulator.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-10 and 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1, 19, 27, and 29 have a limitation of no thin gate oxide, which is found to be indefinite because of the meaning of thin. What would the reference point be to define what thin would be? How thick would an oxide be to be not thin?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-10, 19, 23, 26, 27, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,623,154 Murakami et al.

3. Referring to claim 1, a field transistor containing no gate insulating layer, (See 112 rejection above), comprising: a well region of a first conductivity type, (Figure 1 #20); a field oxide layer, (Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), for defining an active region, (Figure 1 area of #20), on the well region, (Figure 1 #20); high concentration source and drain regions of a second conductivity type, (Figure 1 #9), separated from each other by a width of the field oxide layer, (Figure 1 #15); a low concentration source region of the second conductivity type, (Figure 1 #7), formed in the well region, (Figure 1 #20), the low concentration source, (Figure 1 #7), region being adjacent to the high concentration source region, (Figure 1 #9), and overlapped by one end of the field oxide layer, (Figure 1 #15); a low concentration drain region of the second conductivity type, (Figure 1 #7), formed in the well region, (Figure 1 #20), the low concentration drain region, (Figure 1 #7), being adjacent to the high concentration drain region, (Figure 1 #9), and overlapped by the other end of the field oxide layer, (Figure 1 #15); and a gate conductive layer pattern formed on the field oxide layer, (Figure 1 #15), the gate

conductive layer pattern, (Figure 1 #17), overlapping parts of the low concentration source and drain regions of the second conductivity type, (Figure 1 #7).

4. Referring to claim 2, a field transistor, wherein the well region, (Figure 1 #20), of the first conductivity type is formed on a high concentration buried region, (Figure 1 #3), of the first conductivity type on a semiconductor substrate, (Figure 1 #1), of the first conductivity type.

5. Referring to claim 3, a field transistor, wherein the well region, (Figure 1 #20), of the first conductivity type is formed on a semiconductor substrate, (Figure 1 #1), of the first conductivity type.

6. Referring to claim 4, a field transistor, further comprising a high concentration diffusion region, (Figure 1 #3), of the first conductivity type formed in the well region, (Figure 1 #20), the high concentration diffusion region, (Figure 1 #3), being separated from the high concentration source region, (Figure 1 #9), of the second conductive type by a predetermined distance.

7. Referring to claim 7, a field transistor, further comprising: a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the gate conductive layer pattern, (Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the high concentration source region, (Figure 1 #9), of the second conductivity type; and a drain electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the high concentration drain region, (Figure 1 #9), of the second conductivity type.

8. Referring to claim 10, a field transistor, wherein the first conductivity type is p-type, and the second conductivity type is n-type, (Figure 1).

9. Referring to claim 19, a semiconductor device containing no thin gate insulating layer, (See 112 rejection above), comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), located over a portion of the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type concentration lower, (Murakami et al. Figure 1 #7), than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type concentration lower, (Murakami et al. Figure 1 #7), than the first drain region, (Murakami et al. Figure 1 #9), the second drain region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); and a conductive layer, (Murakami et al. Figure 1 #17), formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7).

10. Referring to claim 23, a device, further comprising: a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the conductive layer, (Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first source region, (Figure 1 #9); and a drain electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first drain region, (Figure 1 #9).

11. Referring to claim 26, a device, wherein the first conductivity type is p-type and the second conductivity type is n-type, (Figure 1).

12. Referring to claim 27, a semiconductor device containing no thin gate insulating layer, (See 112 rejection above), comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), located over the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type, (Murakami et al. Figure

1 #7), concentration lower than the first drain region, (Murakami et al. Figure 1 #9), the second drain region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region underlying the field oxide layer, (Murakami et al. Figure 1 #15); a conductive layer formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7); a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the conductive layer, (Murakami et al. Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first source region, (Murakami et al. Figure 1 #9); and a drain electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first drain region, (Murakami et al. Figure 1 #9).

13. Referring to claim 29, a system for electrostatic discharge protection containing a field transistor without a thin gate insulating layer, (See 112 rejection above), the field transistor comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15 and Col. 8 Lines 27-29 where the gate oxide layer is made by thermal oxidation, which is the same method of making as an isolation FOX layer), located over the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having

a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first drain region, (Murakami et al. Figure 1 #9), the second drain region formed, (Murakami et al. Figure 1 #7), in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); and a conductive layer, (Murakami et al. Figure 1 #17), formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
5/12/04

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800